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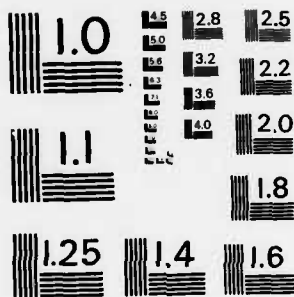
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MICROBUS



DONALD B. BRICK

JULY 1983

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Prepared for

ELECTRONIC SYSTEMS DIVISION  
AIR FORCE SYSTEMS COMMAND  
DEPUTY FOR DEVELOPMENT PLANS  
HANSCom AIR FORCE BASE, MASSACHUSETTS 01731

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"This technical report has been reviewed and is approved for publication."

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REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM										
1. REPORT NUMBER ESD-TR-83-201	2. GOVT ACCESSION NO. AD-A132-338	3. RECIPIENT'S CATALOG NUMBER										
4. TITLE (and Subtitle)  MICROBUS		5. TYPE OF REPORT & PERIOD COVERED										
		6. PERFORMING ORG. REPORT NUMBER										
7. AUTHOR(s)  DONALD B. BRICK		8. CONTRACT OR GRANT NUMBER(s)  IN-HOUSE										
9. PERFORMING ORGANIZATION NAME AND ADDRESS Deputy for Development Plans (XR) Electronic Systems Division Hanscom AFB, MA 01731		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS  N/A										
11. CONTROLLING OFFICE NAME AND ADDRESS Deputy for Development Plans (XR) Electronic Systems Division Hanscom AFB, MA 01731		12. REPORT DATE July 1983										
		13. NUMBER OF PAGES 14										
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		15. SECURITY CLASS. (of this report) UNCLASSIFIED										
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE N/A										
16. DISTRIBUTION STATEMENT (of this Report)  Approved for Public Release; Distribution Unlimited.												
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)												
18. SUPPLEMENTARY NOTES												
19. KEY WORDS (Continue on reverse side if necessary and identify by block number)												
<table border="0"> <tr> <td>STANDARD ELECTRONIC MODULES</td> <td>PRINTED CIRCUIT BOARDS</td> </tr> <tr> <td>MICROBUS</td> <td>BACK PLANES, LSI, VLSI, VHSIC</td> </tr> <tr> <td>PREPLANNED PRODUCT IMPROVEMENT</td> <td>FORM, FIT, FUNCTION</td> </tr> <tr> <td>RELIABILITY AND MAINTAINABILITY</td> <td>ELECTRONIC MODULES</td> </tr> <tr> <td>STANDARD PACKAGING &amp; COOLING</td> <td>LOCAL AREA NETS</td> </tr> </table>			STANDARD ELECTRONIC MODULES	PRINTED CIRCUIT BOARDS	MICROBUS	BACK PLANES, LSI, VLSI, VHSIC	PREPLANNED PRODUCT IMPROVEMENT	FORM, FIT, FUNCTION	RELIABILITY AND MAINTAINABILITY	ELECTRONIC MODULES	STANDARD PACKAGING & COOLING	LOCAL AREA NETS
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<p>Microbus is a technique designed to offer the advantages of Standard Electronic Modules (SEMs) without the disadvantages or shortcomings vis-a-vis Air Force objectives. The Air Force desires the logistic supportability standardization advantages of SEMs without the constraints of fixed function and suppression of the capability to evolve technologically, i.e. to maintain form and fit and relax the constraint on function. Microbus offers a way to accomplish this in modern circuitry using bus structures to replace back planes or wiring</p> <p style="text-align: right;">(continued)</p>												

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20. ABSTRACT (concluded)

harnesses and in fact proposes to extend the buses on to the PC boards, sub-boards or daughter boards and even on to IC chips.

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## 1. INTRODUCTION, THE ROOTS OF MICROBUS

The roots of Microbus lie in the abortive efforts made to implement Standard Electronic Modules (SEMs) in the Air Force, their shortcomings, and the desire to preserve the capability to accomplish evolutionary design or Preplanned Product Improvement (P<sup>3</sup>I). The Navy has been the major prime mover and has implemented a SEM program. The Standard Electronic Module approach has both good and bad attributes.

Some of the good qualities are:

- The achievement of component, board, and/or functional commonality

- Logistic supportability

- Standard documentation

- Standard interfaces

- Reliability

- Standard stock numbers

- Potential savings in spares and O&M dollars as well as test-and-repair costs, personnel & equipment. (The standardization of modules could lead to the wider use of computer-aided test equipment.)

- Reduced dependence on individual suppliers

- Reduced development & acquisition costs (especially through the application of CAD/CAM technology)

- The economies of larger production runs and longer availability of parts

- The wider application of standard packaging & cooling techniques

It is often suggested that a throwaway philosophy might result from the adoption of a SEM process because of the resulting lowered costs of the modules resulting from larger mass production economies.

One of the questions that has to be studied is at what level modularity should be considered, e.g. rack, board, sub-board, etc.

Some of the bad news about SEMs are:

- The Navy's results to date have been mixed:

- About 20 suppliers have been involved. Instead of a few, there are many board sizes (i.e. form factor growth, see Fig. 1). Thus, stocking has been a problem. The R&M experience has been good but module cost growth has minimized the possibility of a throwaway philosophy and boards are being repaired rather than thrown away. Navy acceptance has been mixed (accepted on ships, not in aircraft) and there are no microwave or RF SEMs (a major gap).



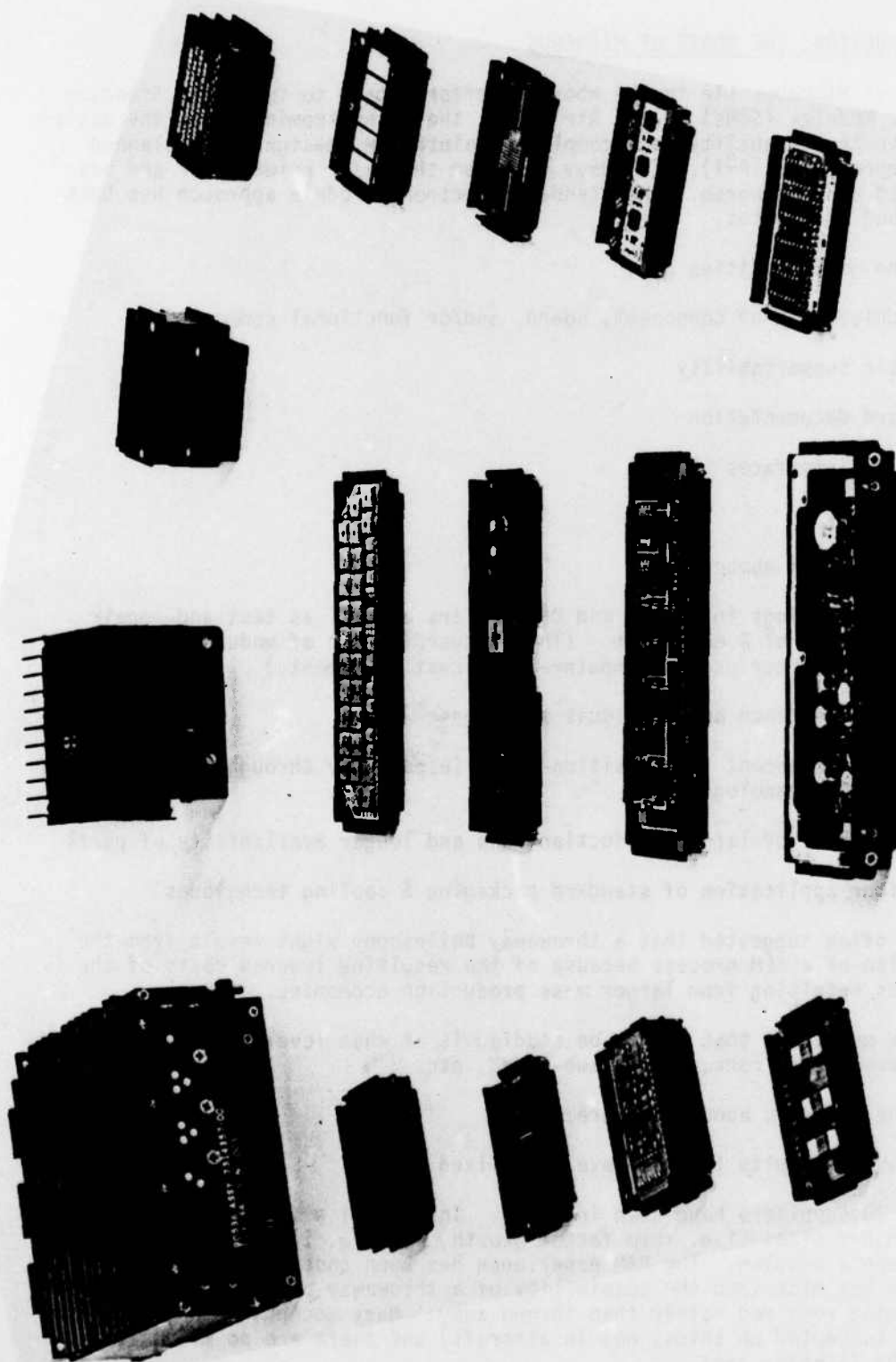


FIGURE 1  
NAVY SEM CONFIGURATIONS

Imposing a SEM standard creates an evolutionary problem, i.e. the imposition of a standard form, fit, and function requirement stifles the application of later technology. This is especially pertinent with respect to LSI, VLSI and VHSIC technologies, as discussed later.

Finally, the workability of a SEM *modus operandi* is in question, e.g. it lacks appeal to circuit designers who don't like to be stifled by fixed form, fit, and function.

The Microbus concept is an approach aimed at gaining the advantages of a Standard Electronic Module approach while at the same time removing the negative aspects.

## 2. THE EVOLUTIONARY PROBLEM

The Microbus approach was stimulated by the desire to allow the standardization of form, fit and function without inhibiting the capability to exploit technological evolution. Basically, the goal was to provide for enhancing a module's functional capability without restricting its backward compatibility or retrofitability. Of the three requirements (form, fit, function), one can think in terms of relaxing 1 or 2 of the 3 constraints, i.e., relax form and maintain fit and function, or maintain function and relax form and fit, etc. as shown below:

~~FORM~~ ~~FIT~~ FUNCTION

~~FORM~~ FIT, FUNCTION

FORM, ~~FIT~~ ~~FUNCTION~~

FORM, ~~FIT~~ FUNCTION

~~FORM~~ FIT, ~~FUNCTION~~

FORM, FIT, ~~FUNCTION~~

The correct choice is to maintain form and fit and relax the constraint on function with the implied potential of enhancing function (e.g. plug-in retrofits or upgrades). The question is, can we accomplish this without precise knowledge of the direction future evolution will take?

The objective is to take advantage of evolutionary improvements which would result in size, weight, electrical power, and/or cost reductions and/or added functional power (additional functions in the same or a reduced envelope).

Presently, physical conditions impose limitations on the freedom to choose which constraints are relaxed. These are illustrated in Fig. 2 where modularity is assumed as the printed circuit (PC) board level. In this case, 'form' is represented by the configuration of the PC board, 'fit' by the PC board pin layout, and 'function' is the operation (or function) performed by the PC board. The left hand column symbolizes J - PC boards performing functions  $F_1, F_2 \dots F_j \dots F_J$  plugged into a back plane or wiring matrix. As evolution reduces the size of the components required to perform the individual functions, the designer has the choice of:

Leaving unused or wasted space on the resulting PC boards preserving form, fit, and function (top line of Fig. 2),

# EVOLUTION AND BACKWARD COMPATIBILITY

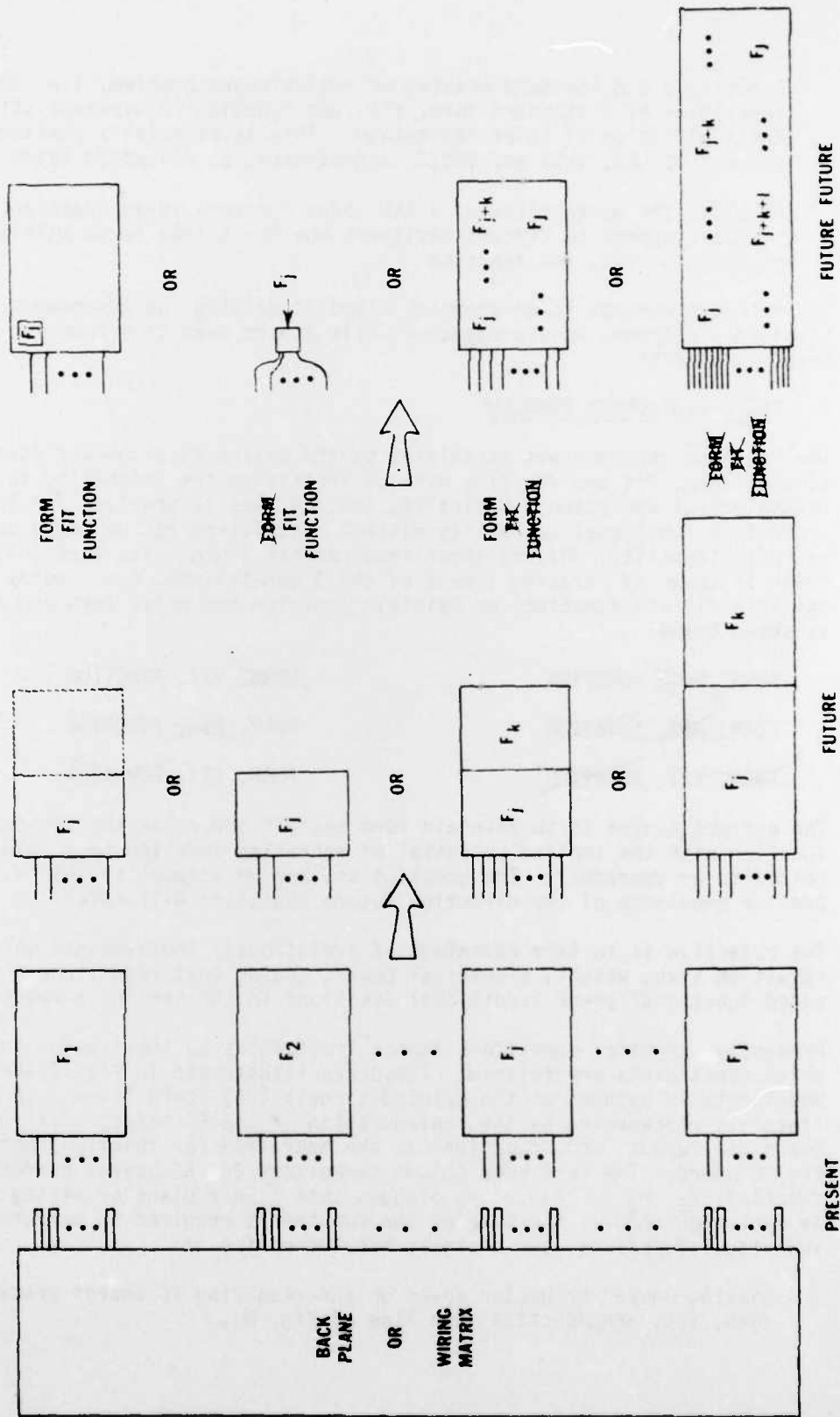


FIGURE 2

Reducing the board size thereby violating the fixed 'form' factor of the SEM concept (second line of Fig. 2),

Adding additional function(s) and preserving board size (third line), violating the fixed 'function' factor (a desirable trait); however, unless one had the foresight to provide sufficient additional pin connections on the original board and back plane, the resulting pin-out must be changed thereby fixed 'fit' is also violated, as shown. Thus, it is virtually impossible with this configuration to achieve fixed form and fit with enhanced function.

Finally, one could violate all three: form, fit, and function. Note that as with the third case, unless one possessed infinite foresight in providing a sufficient number of pins and richness of back plane connectivity, the course of evolution would not be backward compatible.

Fig. 3 further indicates what is desired of evolution. In the near future, the objective is to reduce the number of boards. Later, more functionality is to be added with the same number of boards as the original system had. In both cases, form is preserved, overall system function is either preserved or enhanced, but fit is violated unless one has had either infinite foresight or adopted an alternate strategy. Microbus is such an alternate strategy.

### 3. THE CONCEPT OF MICROBUS

Microbus proposes to replace the back plane, or wiring matrix, or harness with a bus structure composed of one or more electrical buses. Furthermore, it will be seen that it may be profitable to continue the buses on to the PC boards and interface to the bus(es) at a sub-board level rather than provide bus interfaces to the electronics on the board at the board level. This is illustrated in Fig. 4, the analog of Fig. 2, where the same alternatives as in Fig. 2 are shown with, however, the back plane or wiring harness replaced by a bus (illustrated as a two-wire line for simplicity). Note that it is now possible (third line of figure) to achieve fixed form and fit while providing for enhanced function. The right hand column of Fig. 4 shows how the bus might be extended on to the PC boards and indicates that bus interfacing might be done at a sub-PC board level.

In summary, the Microbus concept involves a bus structure replacing the back plane, wiring matrix, or wiring harness in conventional PC board module configurations. The bus structure can extend on to the PC boards themselves. Furthermore, the buses can extend on to daughter boards. The bus structure can even extend on to IC chips and ad infinitum. This is illustrated in Fig. 5, the analog of Fig. 3, which illustrates not only how the bus structure can extend on to the boards, sub-boards, etc. but also how additional functions can be added in the future in the same package size (or the same functions in a smaller package) and how parallel buses can be added if bus traffic so requires (right hand column). If in fact, a sufficiently rich bus interface unit to handle multiple buses was not included originally, bus relays can be included in later boards to handle this, as shown in the right hand column. The continued reduction in size and cost of digital electronics allows the overhead of bus interface units, relays, etc. to be supported with little

# EVOLUTION AND ENHANCED FUNCTION PLUS BACKWARD COMPATIBILITY

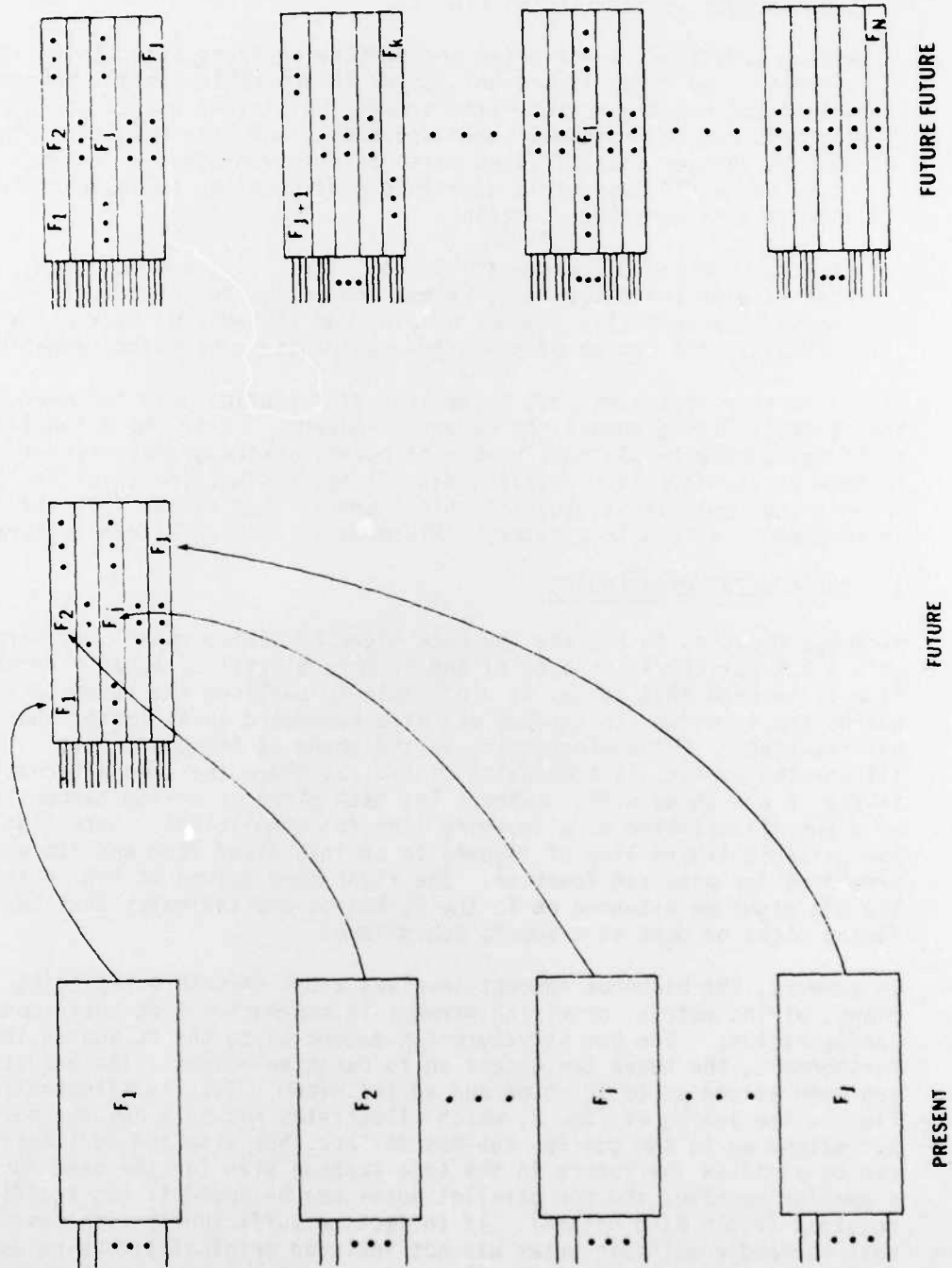


FIGURE 3

# EVOLUTION AND BACKWARD COMPATIBILITY WITH MICROBUS

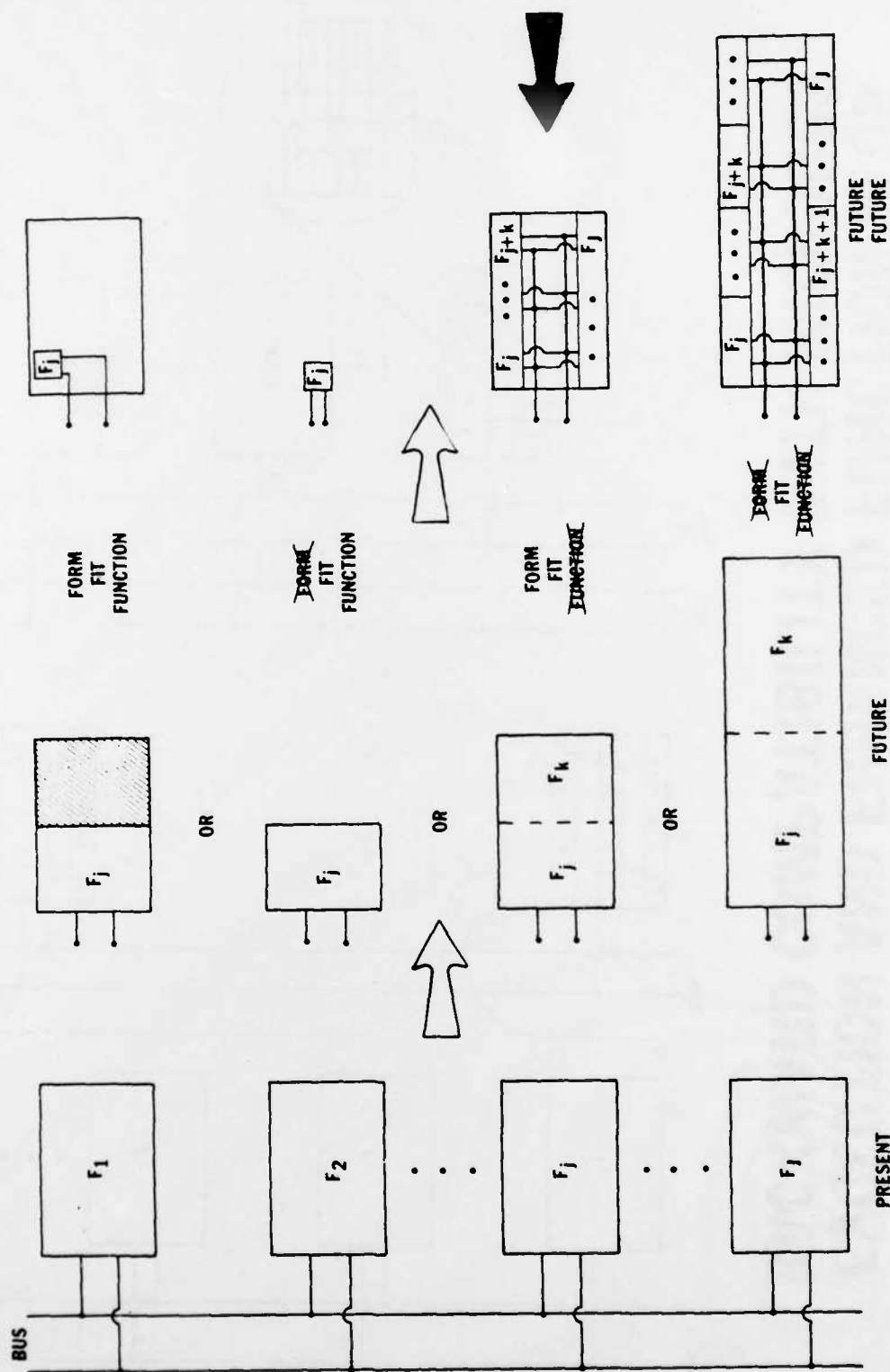


FIGURE 4

# EVOLUTION AND ENHANCED FUNCTION PLUS BACKWARD COMPATIBILITY WITH MICROBUS

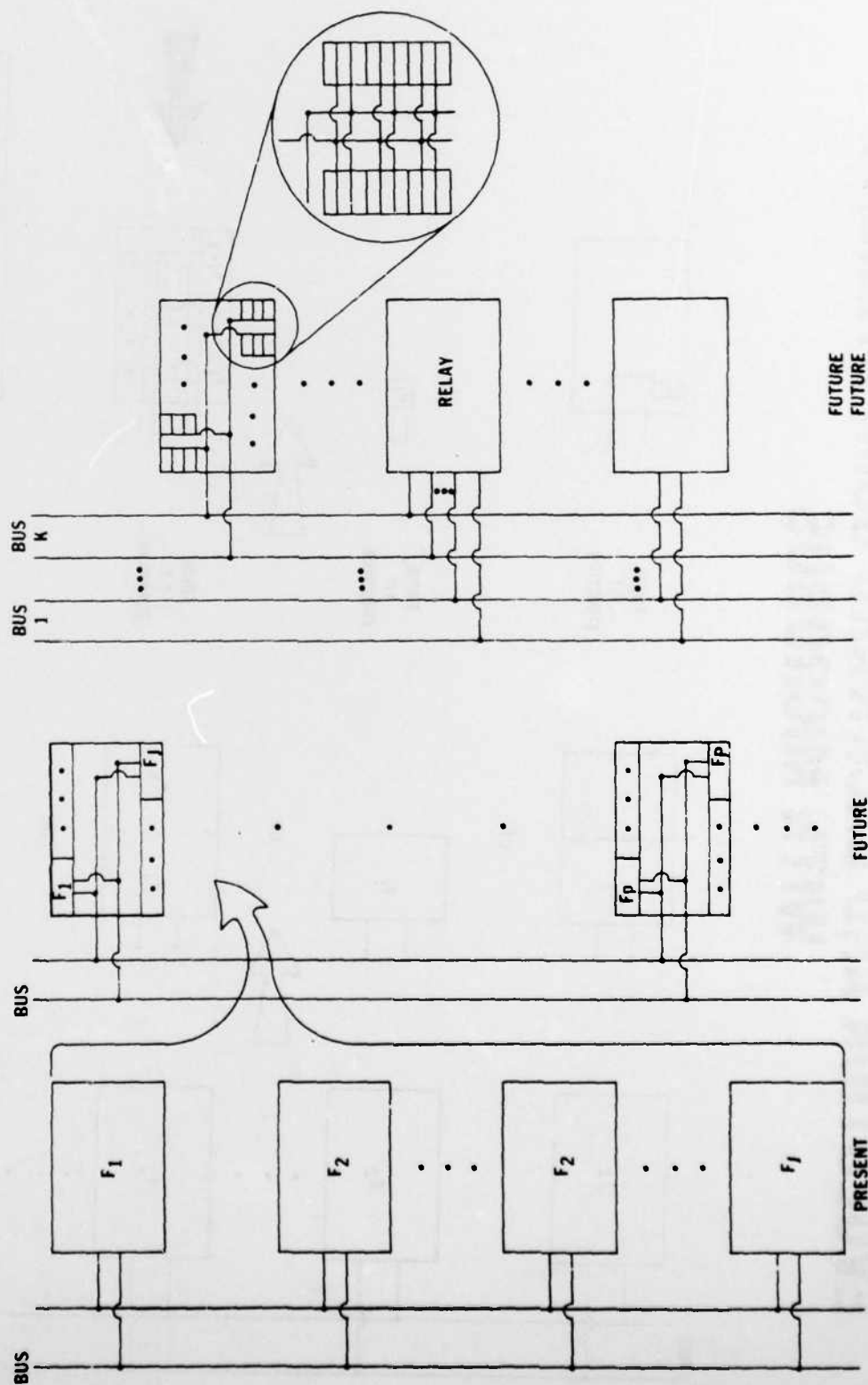


FIGURE 5

penalty. The Microbus process does not require predicting the direction of evolution before it occurs to accommodate additional board and/or system functions (back planes, connectors, wires, etc.). It facilitates growth and evolution consistent with form, fit, function (functional growth), and modularity at the board (or lower) level. As mentioned before, the penalty is the use and management of buses and bus interfaces.

#### 4. ADDITIONAL FEATURES OF MICROBUS

In harmony with local area net (LAN) architectures\* (in particular flexible intraconnect (FI) LAN).

Consistent with the trend in the computer industry toward bus-architected back planes (e.g., Multibus (Intel), Unibus (DEC), STD (Manufacturers Industry Association)).

Could provide impetus to extending buses on to chips including custom LSIs and VHSICs/VLSICs. With regard to the latter, architectural guidance is needed, and some contractors are thinking along these lines already.

Microbus can exploit the advantages of fiber optic buses. It is fully evolutionary to opto electronics and optical processing.

#### 5. RECOMMENDATIONS

As a result of this work, it was recommended that the Air Force initiate a 6.2/6.3 program to investigate the feasibility and technology of the Microbus approach, consisting of:

A feasibility study

An application study to determine where Microbus is applicable, recommend at what level(s) modularity should be applied, the pros/cons and cost impacts thereof and to determine if BITE/BITAF\*\* could be accomplished and at what levels.

A detailed architectural study for various applications

Develop Air Force architectural standards including specifications for bus management

An investigation of design modifications to, and interfaces with:

Higher levels (back planes)

Sub levels (e.g., VHSIC chips)

RADC and AFWL/AA were briefed on this program. A joint study was recommended with RADC leading most of the study but with the Avionics Laboratory handling the VHSIC/sub-level portion. These recommendations are in the process of being implemented.

\*Being applied to C<sup>3</sup>I, communication process and machine control, office administrative, management, business, etc. systems.

\*\*Built-In Test and Built-In Test and Fix



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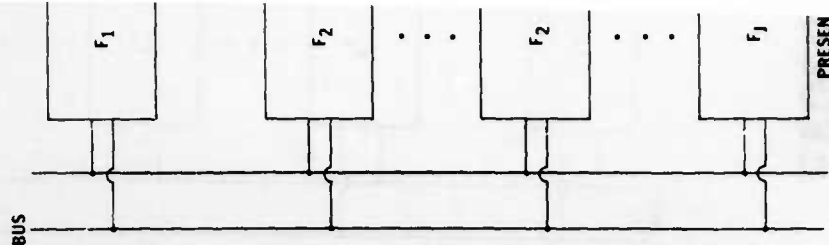
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*Joseph D. Morgan 3*  
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Deputy for Development Plans

# EVOLVING BACKWARD



RADC and AFML/AA were oriented on this program. A joint study with RADC leading most of the study but with the Avionics Laboratory handling the VHSIC/sub-level portion. These recommendations are in the process of being implemented.

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